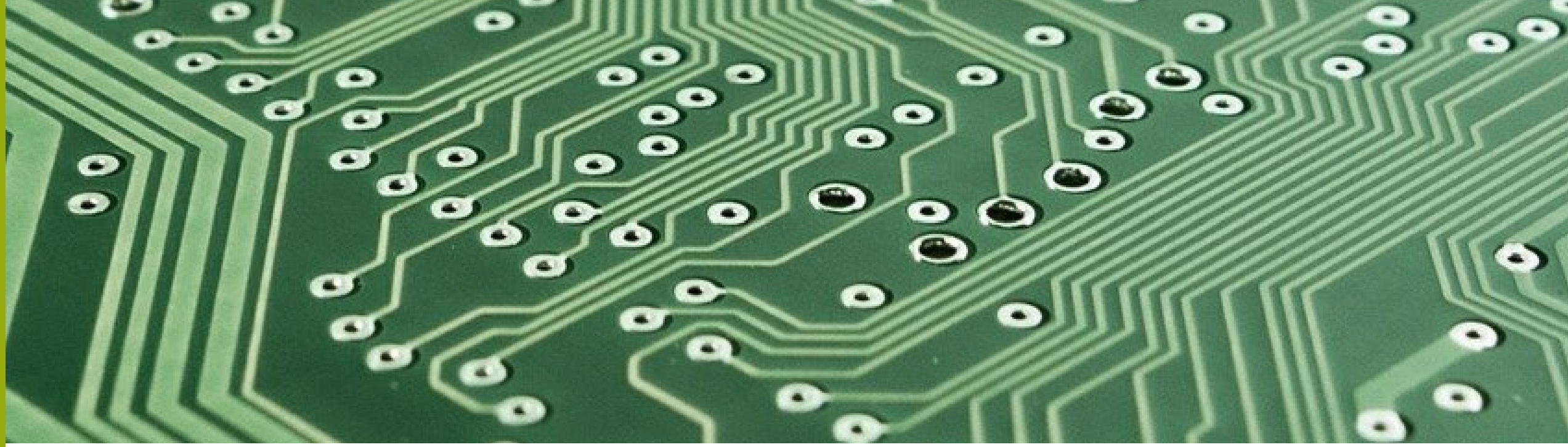


Experimenting with Open ISAs

and the associated projects, toolchains, devices, etc.

Agenda

1. Who am I ?
2. OpenPOWER and RISC-V
3. Exploring OpenPOWER
4. Microwatt Usage
5. FPGAs
6. General Resources & Roadmap

Who am I?

Background

Electrical and Electronics Engg Senior, NIT Karnataka

Research Assistant, CAD Lab, IISc Bengaluru

Google Summer of Code '20, FOSSi Foundation

Summer Intern (2019), IIT Bombay

Interests

- Digital Design
- Computer Architecture
- FPGAs
- Embedded Systems
- Open-source

OpenPOWER and RISC-V

OpenPOWER ISA

- IBM 801 was one of the first RISC computers
- RISC System/6000 (1990) introduced POWER ISA
- IBM + Apple + Motorola (AIM Alliance) worked on PowerPC
- Renamed as POWER ISA in 2006
- OpenPOWER Foundation started in 2013
- Latest Spec Version - 3.1

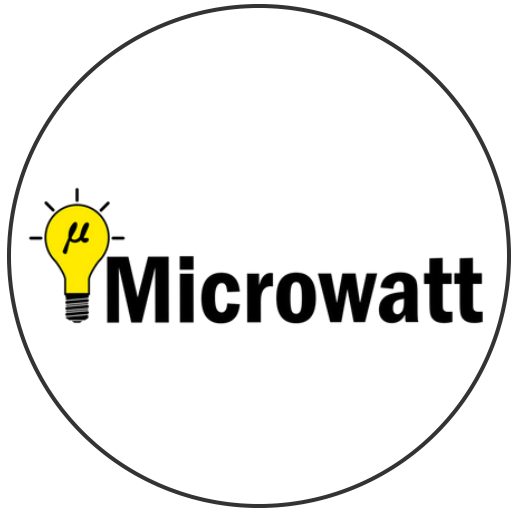
  (Used in POWER10)

RISC-V

- 5th RISC ISA from Berkeley (2010)
- Open right from the beginning
- Maintained and promoted by RISC-V International
- Adopted by SiFive, WD, Nvidia, Microchip, Alibaba, CDAC, IIT Madras

Exploring OpenPOWER

Open Source POWER Cores



Microwatt

VHDL 2008

GHDL Simulator

Xilinx FPGAs (A7)

Also supported in LiteX, FuseSoC

Chiselwatt

Chisel

Verilator Simulator

Yosys/nextpnr support for ECP5 based FPGAs

(ULX3S / Orangecrab etc.)

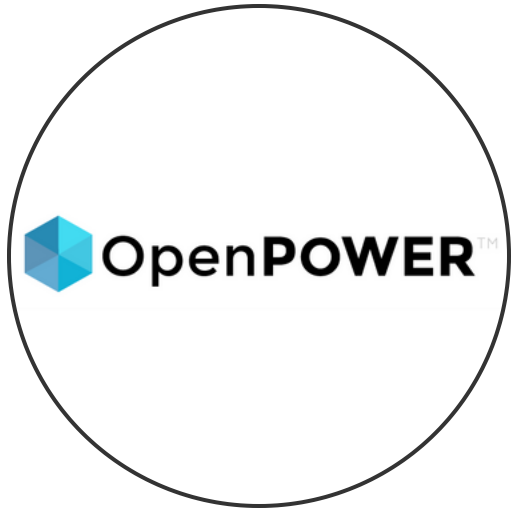
A2I

VHDL

POWER ISA v2.06 compliant

4 way multithreaded, in-order, 16+16 kB I$/D$

Used in BlueGene/Q



A2O

Verilog

POWER ISA v2.07 compliant

Modern than A2I, 2-way MT, OoO, 32+32 kB I$/D$

Microwatt Usage

All steps also available in detail at blog.shivampotdar.me | Interactive ASCII cinema

1. Clone the repo! - gh/antonblanchard/microwatt
2. Install PowerPC cross-toolchain.
3. Build Micropython and GHDL
4. Build Microwatt
5. Write and compile your code -> Link to main_ram.bin
6. Go!

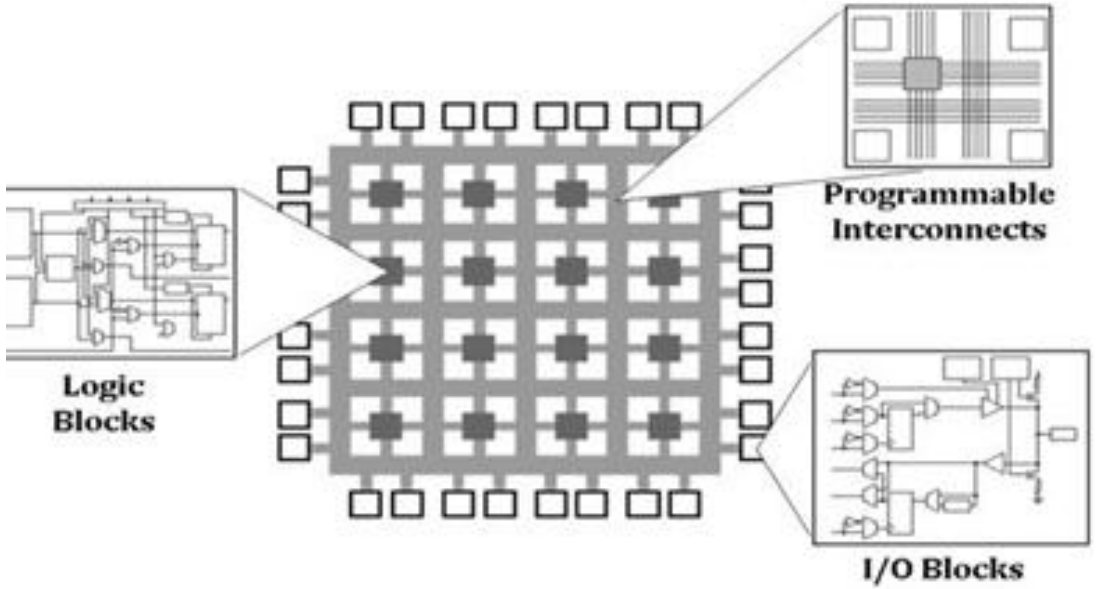
```
ubuntu@ip-172-31-84-201:~/uwatt/microwatt$ ./core_tb > /dev/null

   .oOOo.
 ."      ".
 ;  .mw.  ;   Microwatt, it works.
  .  '  '  .
   \ || /
    ;..;
    ;..;
    `ww'
```

```
ubuntu@ip-172-31-84-201:~/uwatt/microwatt$ ./core_tb > /dev/null
MicroPython v1.12-571-g16d6cb7f7-dirty on 2020-06-23; bare-metal with POWE
RPC
Type "help()" for more information.
>>> 1+2
3
```

```
ubuntu@ip-172-31-84-201:~/uwatt/microwatt$ ./core_tb > /dev/null
0
 1
  3
   6
    10
      15
        21
          28
            36
              45
                55
                  Shivam
```

FPGAs



- Programmable and reconfigurable hardware
- Code -> Actual digital logic!
- Configurable logic blocks (CLBs) connected with programmable interconnects
- FSM, CPU, SoC, GPU - everything can be modelled!
- You can boot Linux on an FPGA!

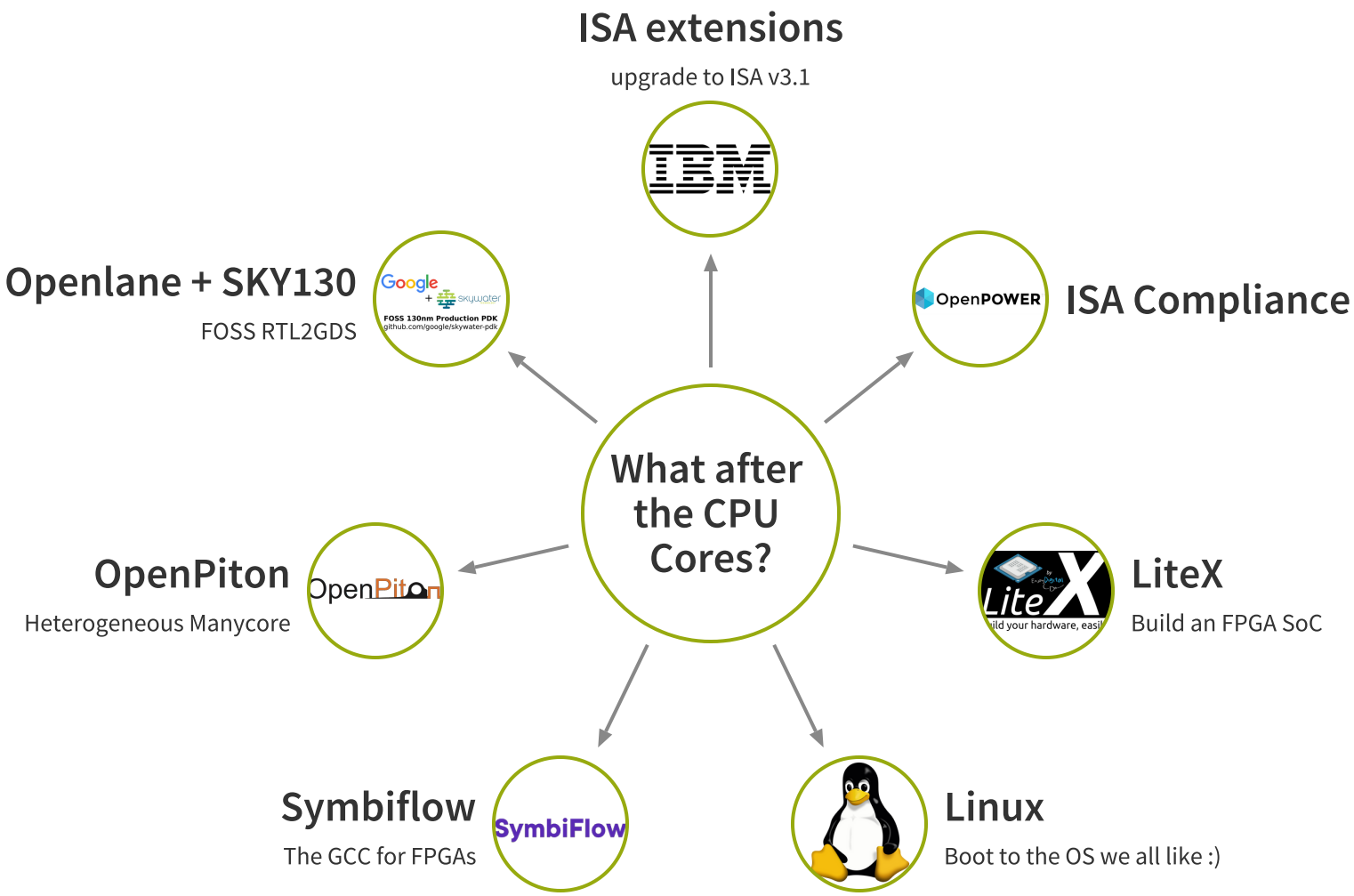
FPGAs ..

- **Advantages**
  - Reconfigurable
  - Highly versatile and flexible
  - Massively parallel
  - Large I/O count
  - Very fast
  - Lesser time to prototype / market
- **Disadvantages**
  - Expensive
  - High power consumption
  - Comparatively steep learning curve
  - (Traditionally) complex toolchains
  - Verilog / VHDL non intuitive

FPGAs and Open-Source

- OSHW - RTL and surrounding software
- FPGAs - accessible to anyone / anywhere
- Expensive toolchains ? -> Symbiflow
- Expensive hardware? -> ECP5
- Complex HDLs? -> Chisel, Migen (& LiteX), TL-Verilog
- Beyond FPGAs? -> Skywater PDK!

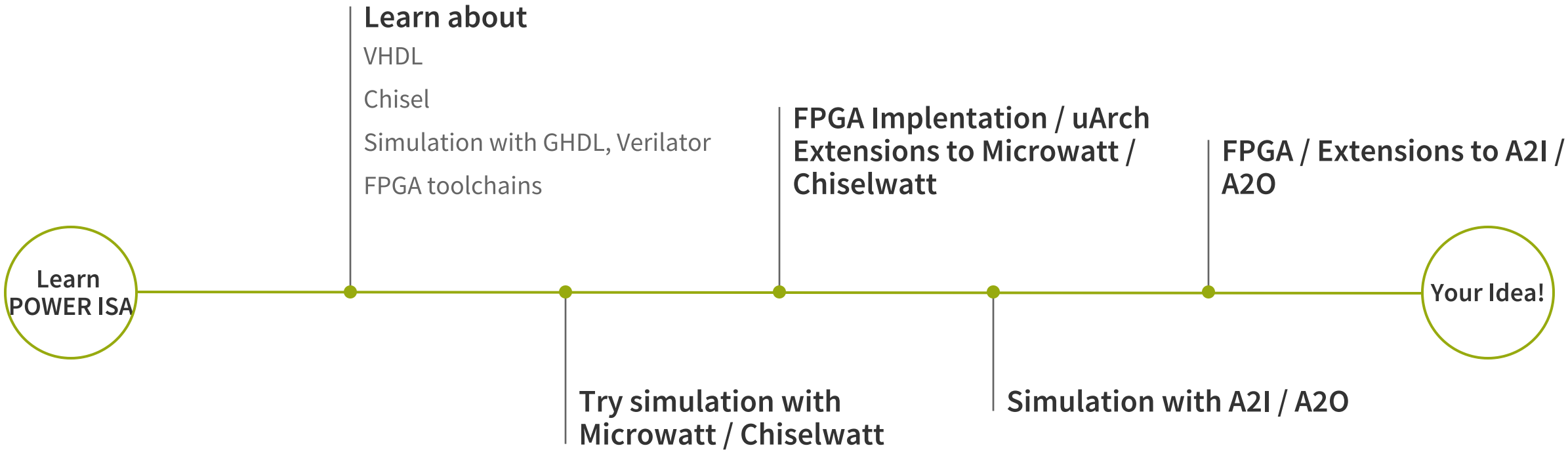
General Resources & Roadmap



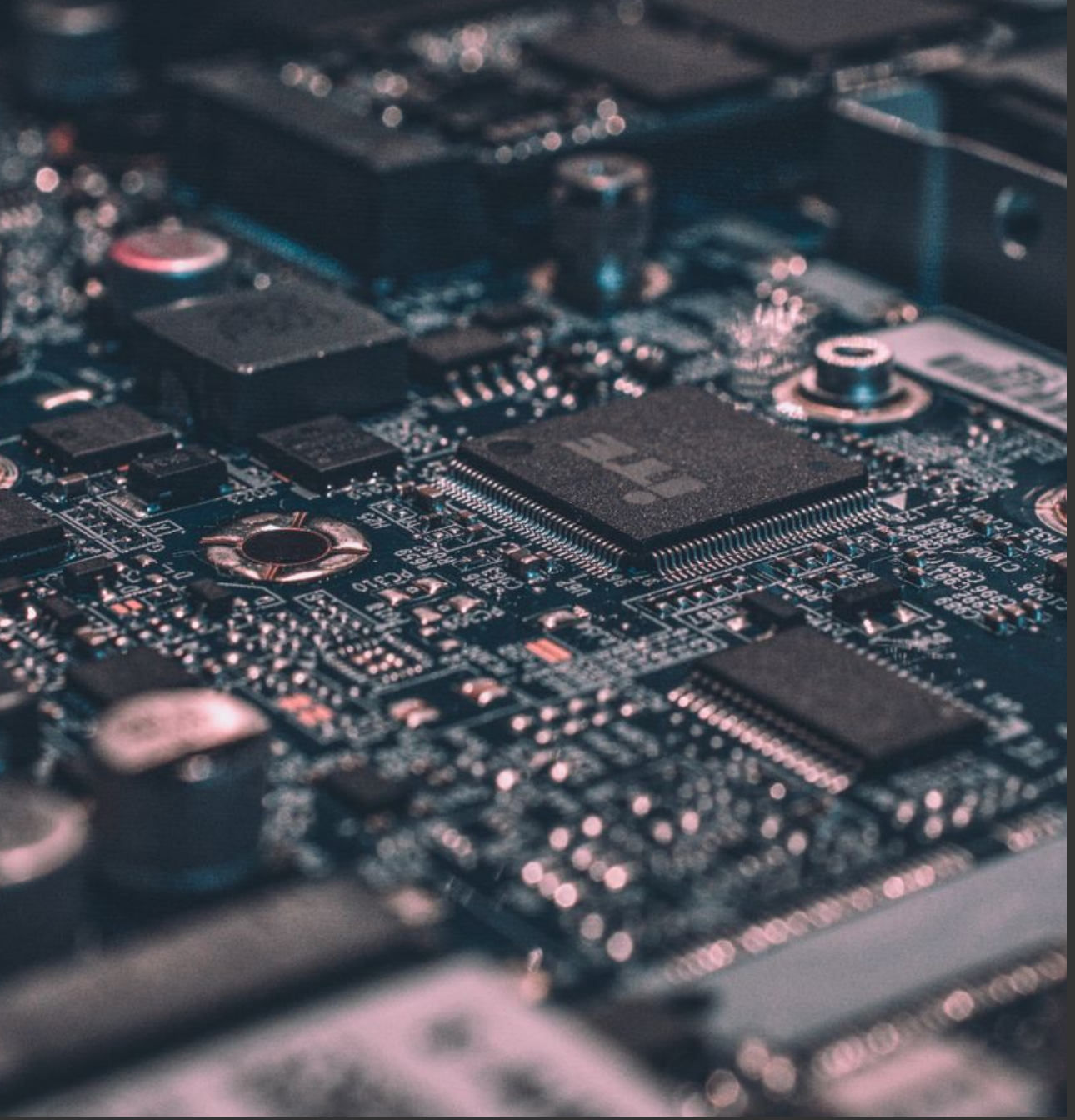
Resources for Beginners

- Computer Organization and Design - Patterson and Hennessy
- POWER ISA Books
- VHDL/ Verilog - books and YouTube videos by Brock J Lamares (Free)
- All 4 cores are available on GitHub
- Verilator, GHDL, Yosys documentation
- Numerous examples and derived projects with open source tools

Potential Roadmap



Questions?



Shivam Potdar

https://shivampotdar.me

shivampotdar99

shivampotdar99@gmail.com

shivampotdar99

+91-9511893050