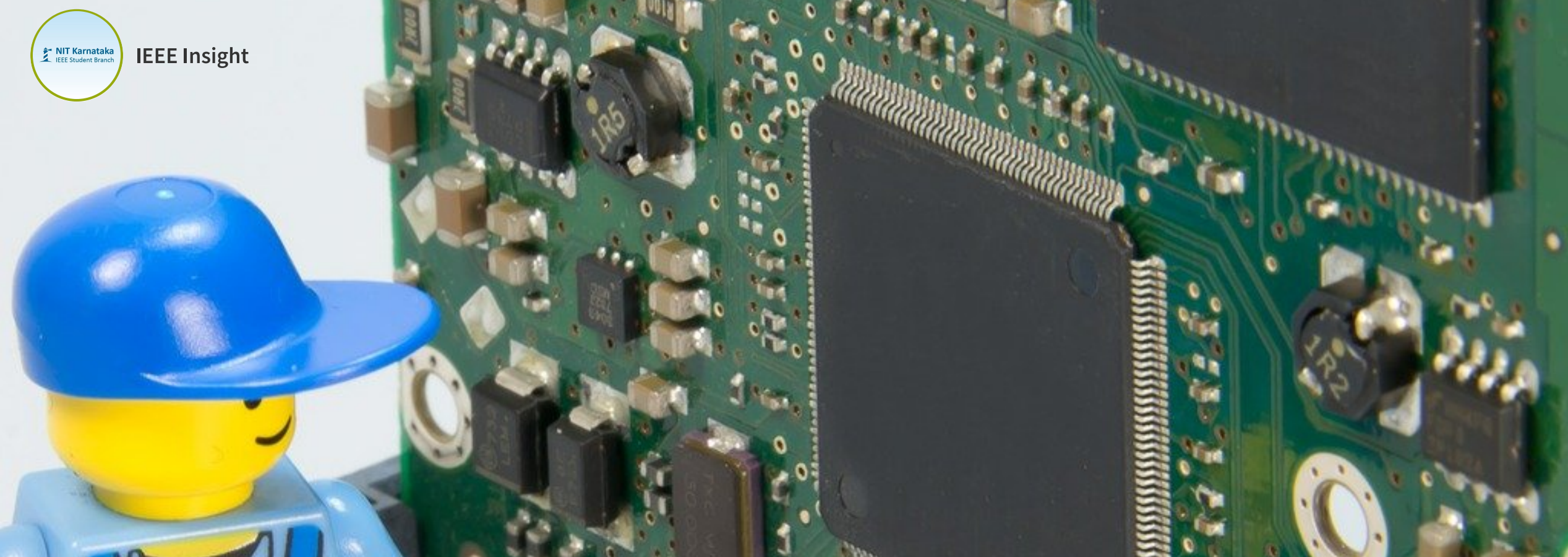




IEEE Insight



Hacking Your Career

with hardware, academics, research and open-source!

Agenda

- 1 Who am I?
- 2 About EE/EC
- 3 My Journey
- 4 Career Options
- 5 General Tips

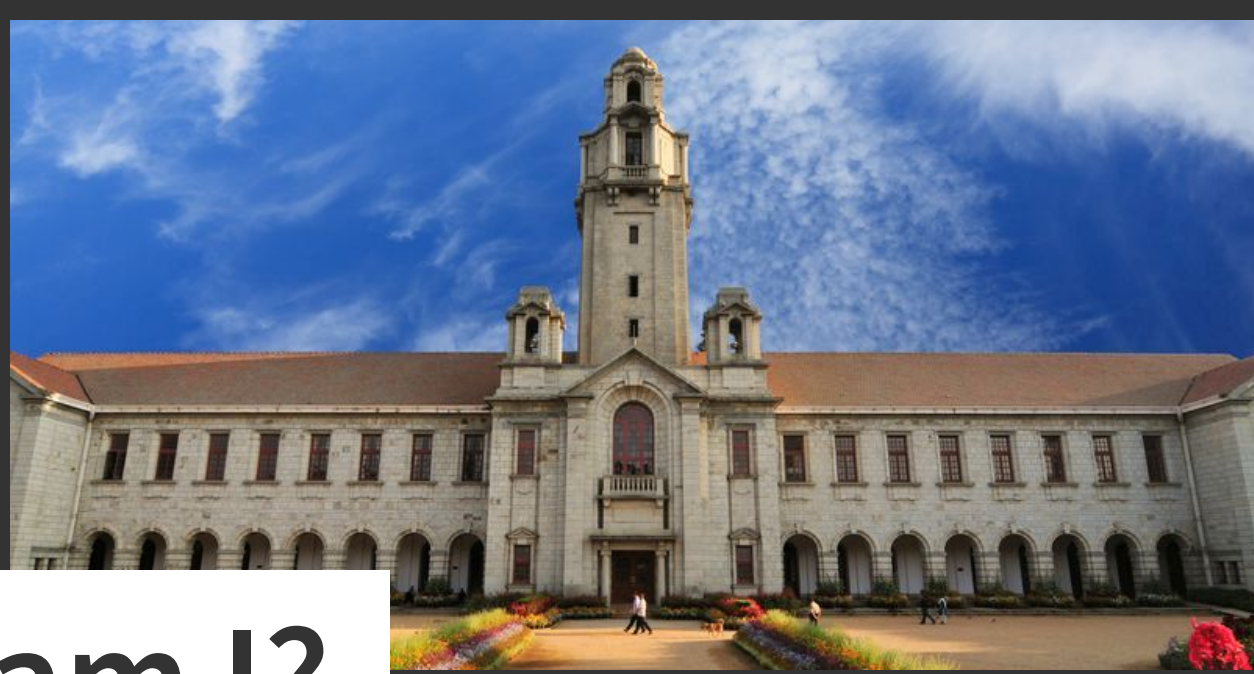


Hacking

Hacking

means

- **(v.) be able to manage successfully**
your NITK life xD
- **(n.) a good solution or piece of advice**
you will definitely get a lot of this today
- **(v.) intrude computers and hardware!**
personal favourite :)



Who am I?



Google Summer of Code

Background

They told you already I believe :)



Sr. Engineer Hardware - Samsung
Semiconductor (India R&D)*



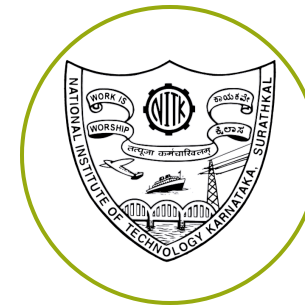
Research Assistant, CAD Lab, IISc
Bengaluru



Google Summer of Code '20,
FOSSi Foundation



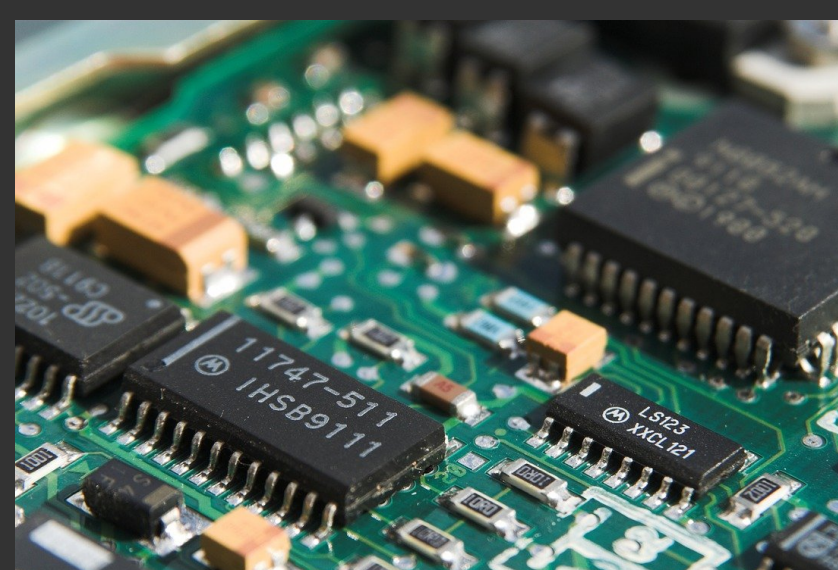
Summer Intern ('19), IIT Bombay



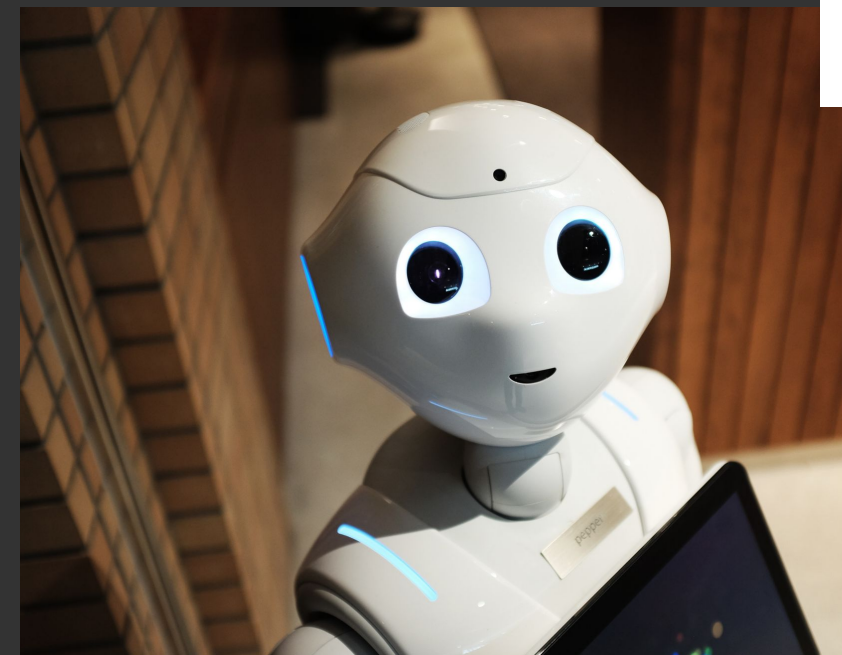
EEE Senior, NITK

Who am I in NITK?

- Finished 159/170 credits in 3 years :)
- Took courses from: EEE, ECE, CSE and CSD
- CGPA: 8.62
- Clubs:
 - ACM
 - Flying and Robotics Club (FARC)
 - IRIS NITK
 - Technites



About EE/EC



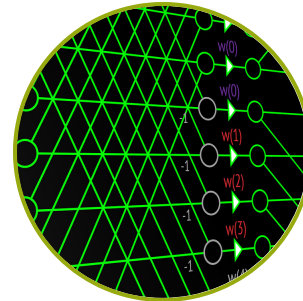
Electrical and Electronics



Power Electronics



Power Systems

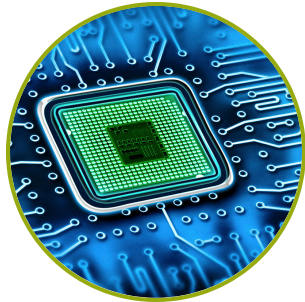


Signal Processing



Control Systems

Electronics and Communication



VLSI (Very Large-Scale Integration)



Communication



Signal Processing and Machine Learning (SPML)



My Journey

First Year

- **C and Python**

C is an NITK course and Python online

- **Linux**

Sooner the better - extremely important in any circuit branch

- **LaTeX**

Levels up your presentation skills

- **Arduino / NodeMCU**

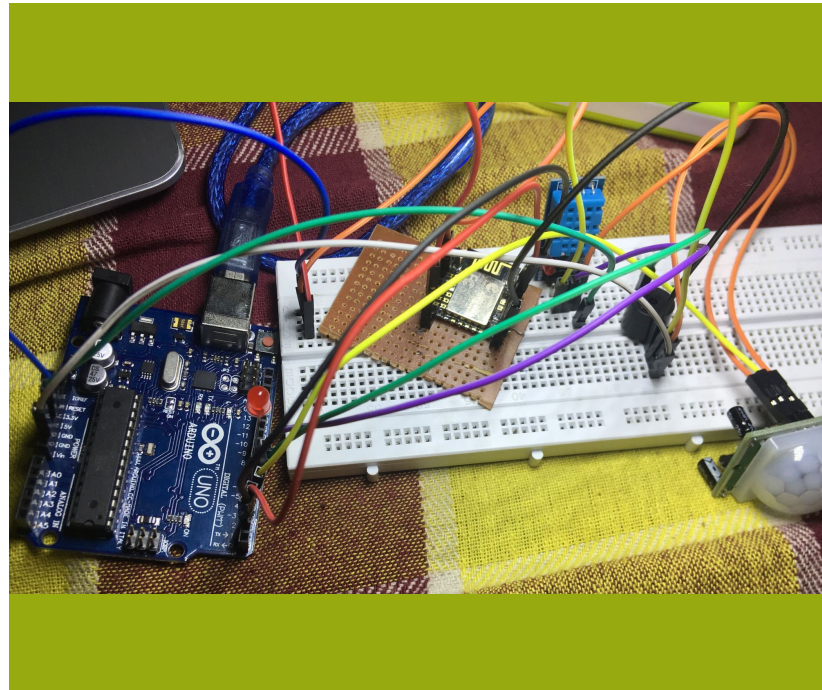
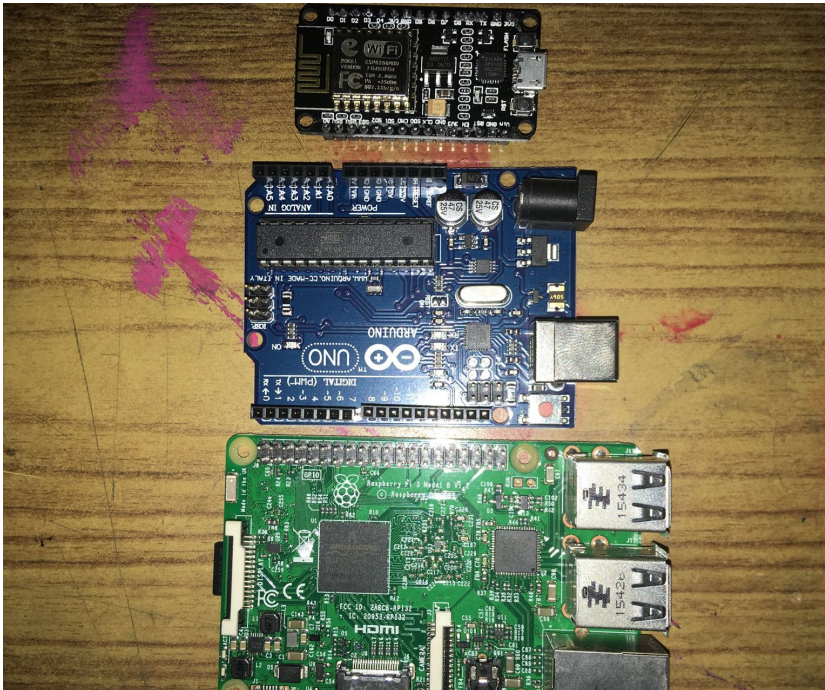
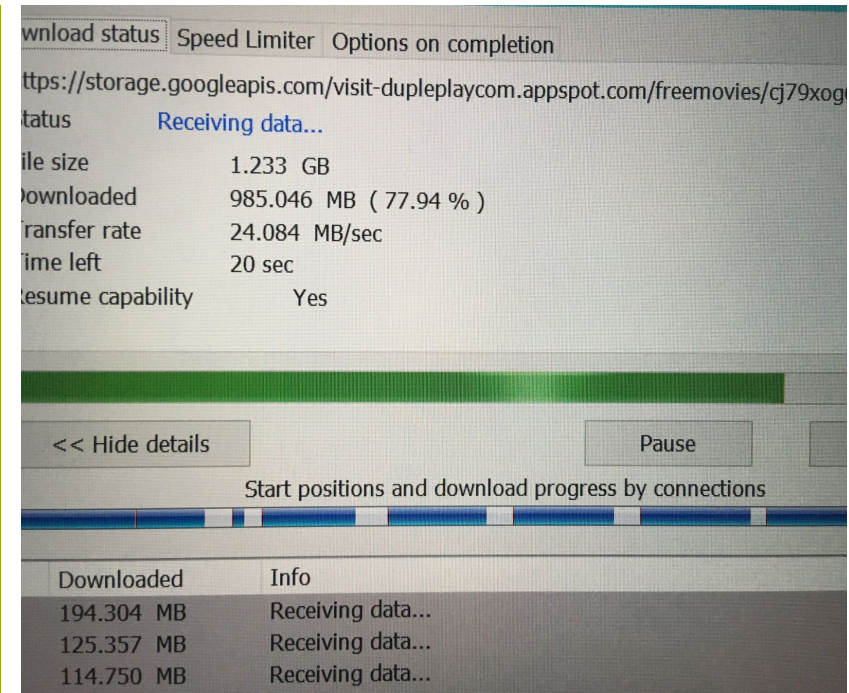
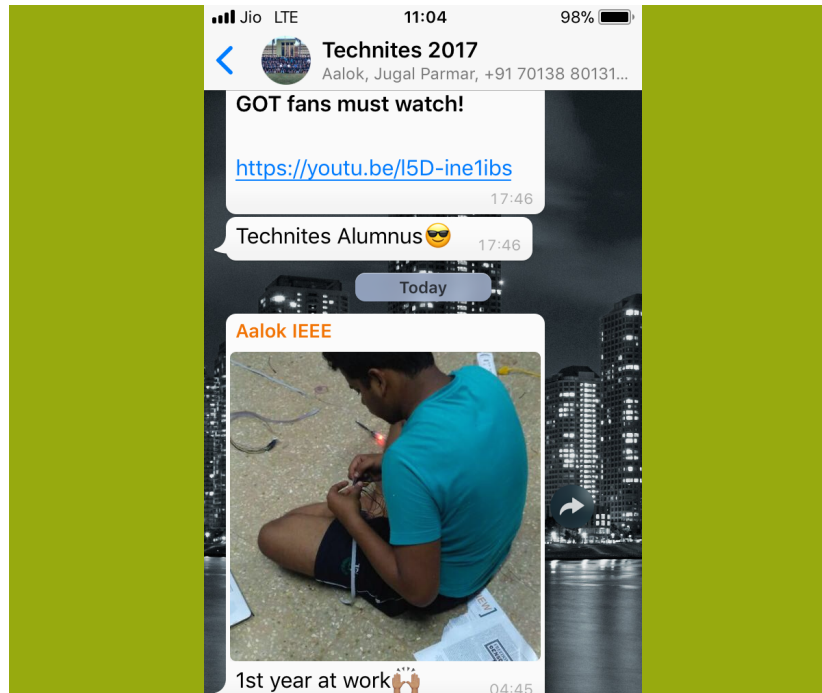
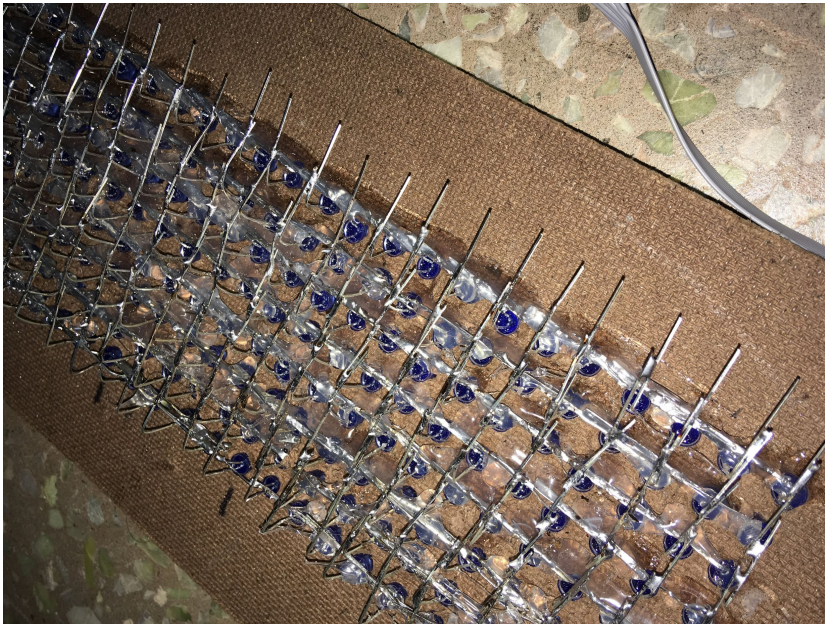
Hello world of electronics

- **Technites**

One of the best places in campus for hands on projects

- **Best Time to Explore**

Friends, Seniors, Mangalore / Manipal, Fests, Institute, Departments, Minors etc.



Second Year

- **Joined ACM, IRIS**

SMP performance helps!

IRIS for Product Management

- **Won a Coding Hackathon**

Based on C/Python and Arduino!

- **Industrial Training on Transformers**

Again: Try them all !

- **eYantra Robotics Competition**

Advanced Embedded Programming, Computer Vision, a bit of mechanical!

- **First course outside EEE**

Open Source Virtual Instrumentation - in CSD

- **Summer Internship at IITB!**



 **NITTE** | **NMAM INSTITUTE OF TECHNOLOGY**
EDUCATION TRUST
(An Autonomous Institution under VTU Belgaum)

****WINNER**** 29 | 09 | 2018

<CH/>

CODING HACKATHON

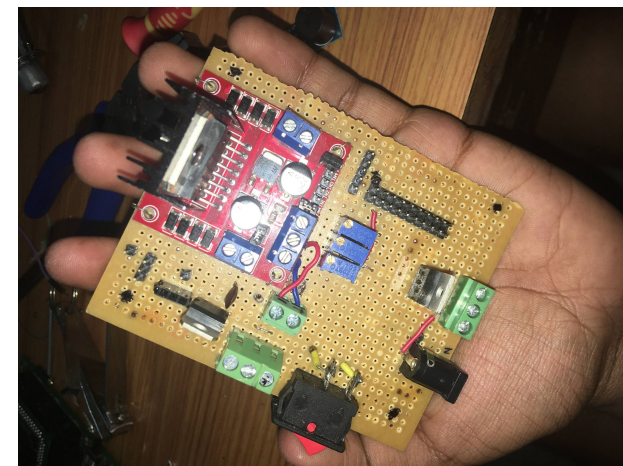
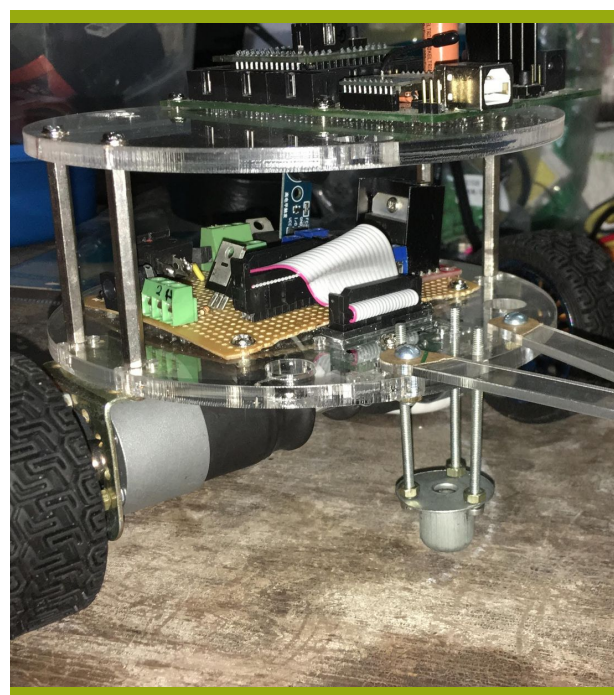
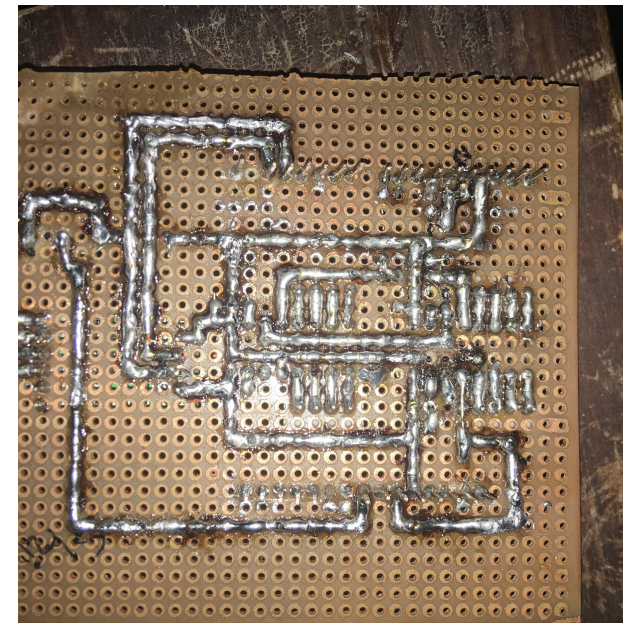
PAY SHIVAM POTDAR

RUPEES ₹10,000/- (TEN THOUSAND RUPEES ONLY)

Winner of 'Coding Hackathon' organised by IoT club under CFSI, In Association with NAIN (A Subsidiary of Dept. of IT, BT and S&T, Government of Karnataka)

   
(Dr. Miranjan N. Chiplun
Principal)

"29-09-2018" 987600076333214 22nd, 23rd & 29th Sept



```
14 architecture alu of alu is
15   signal a_sgn, b_sgn : signed(7 downto 0);
16   signal c_sgn : integer;
17
18 begin -- architecture alu
19   a_sgn <= signed(a);
20   b_sgn <= signed(b);
21   c_sgn <= 1 when c_in='1' else 0;
22   y <= not a when opcode = "0000"
23     else not b when opcode = "0001"
24     else a and b when opcode = "0010"
25     else a or b when opcode = "0011"
26     else a nand b when opcode = "0100"
27     else a nar b when opcode = "0101"
28     else a xor b when opcode = "0110"
29     else a xnor b when opcode = "0111"
30     else a when opcode = "1000"
31     else b when opcode = "1001"
32     else std_logic_vector(a_sgn + 1) when opcode = "1010"
33     else std_logic_vector(b_sgn + 1) when opcode = "1011"
34     else std_logic_vector(a_sgn - 1) when opcode = "1100"
35     else std_logic_vector(b_sgn - 1) when opcode = "1101"
36     else std_logic_vector(a_sgn + b_sgn) when opcode = "1110"
37     else std_logic_vector(a_sgn + b_sgn + c_sgn);
```

External compiler
-- Loading package constants
-- Compiling architecture RTL of dut
-- Compiling entity testbench
-- Compiling architecture STR of testbench
-- Loading entity dut
End time: 20:18:19 on Jun 21, 2019, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
Finished external compiler run



IITB!



Third Year

- **Embedded Systems and VLSI from ECE**

One of the most practical courses I have ever had

- **First significant open-source contribution!**

for e-Yantra, IITB in Hacktoberfest

- **Tried Machine Learning**

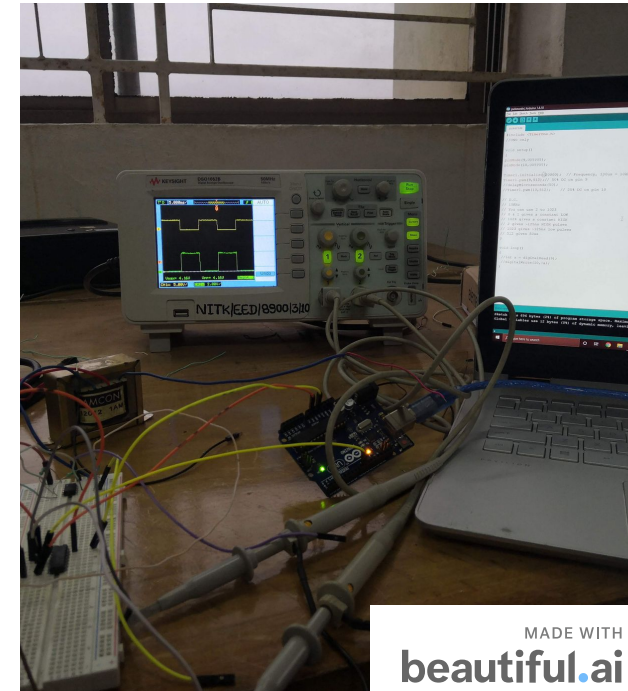
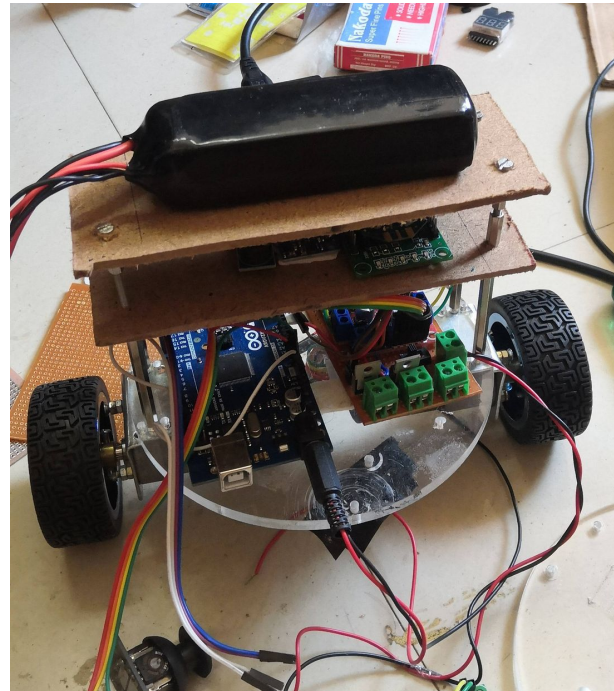
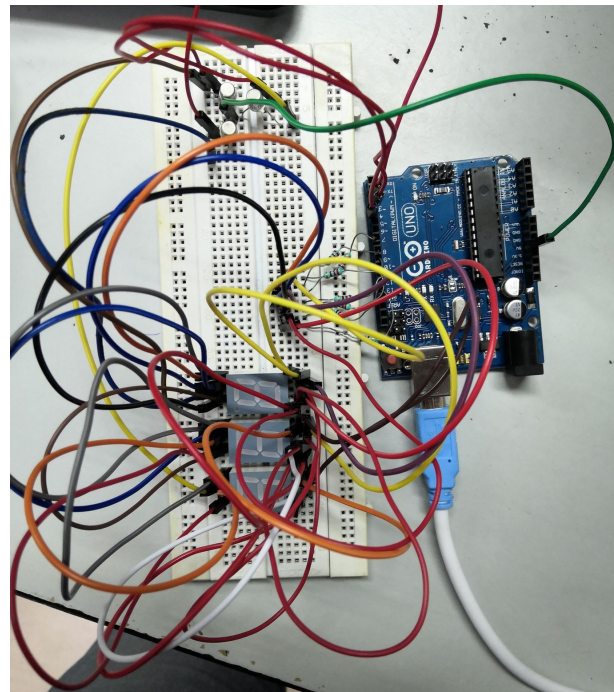
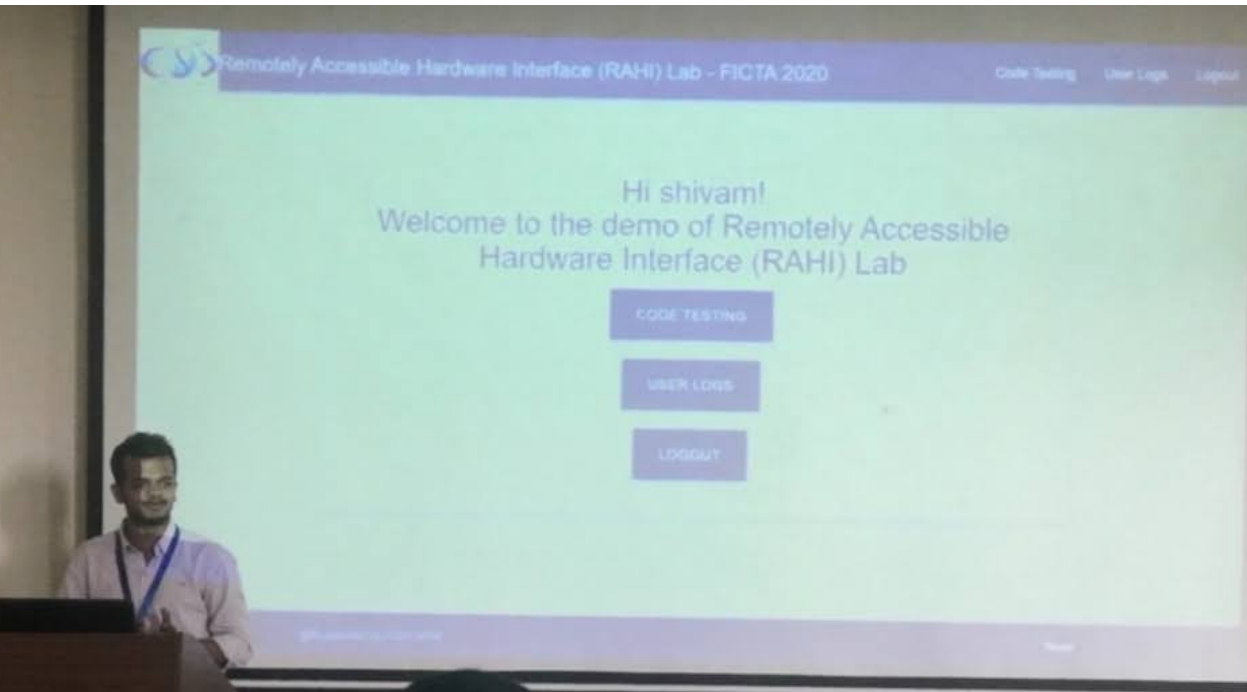
with Winter School on ML in Medical Image Analysis

- **First research paper!**

Evolved from OSVI project

- **Computer Architecture course from CSE**

- **Year-off at IISc!**



Final Year

Ft. COVID-19



- **GSoC**

- Hardware + Open Source + WFH = Perfect 2020 Combo
- Earned first stipend!

- **First presentation in an International Conference**

Virtually :(and attended many more as all were online

- **Placed at Samsung Semiconductor India R&D**

GSoC and IISc experience helped!

- **Teaching Assistant (TA) Experience**

4 workshops with Kunal Ghosh!

- **Made many global connections**

- Open-Source community as a whole is very welcoming!
- Use LinkedIn, Twitter, Reddit, Discord

DAC YF

Flexible Manycore CPU Design with TL-Verilog
 Shivam Potdar (YF), Steve Hoover, Jonathan Balkind (Mentors)



Flexible and Configurable CPU Microarchitecture

TL-Verilog (Timing Abstract)

Params: WordWidth = ..., Config: ISA = ..., Staging: Fetch = 1, Decode = 2, Execute = 3

TL-Verilog + M4 Macros

Verilog (correct by construction with staging, fine-grained clock gating etc.)

Flexible and Scalable Uncore

OpenPiton

BYOC Memory System

DDR Memory, Wishbone SDHC, Ethernet, VGA Framebuffer, UART, Bootrom, Debug Module, CLINT, PLIC, RISC-V specific

Chipset NoC Crossbars

Transaction-Response Interface (TRI)

WARP-V (RISC-V / MIPS / OpenPOWER), PicorV32 Core (RISC-V 32), Athina Core (RISC-V 64), a0486 Core (x86), OpenSPARC T1 Core (SPARC v9)

Huge Code Reduction and Flexibility, but full RTL Control !

Design Stage	Code Reduction (Approximate)
Source	~100%
TL-Verilog	~80%
1-stage	~60%
5-stage	~40%
7-stage	~20%

Legend: Other, Gating, Validity, Structure, Staging, Declarations, Logic, Unstaged

Key Takeaways :

- Demonstrates large-scale design in new Verilog-compatible design and formal verification methodology
- Hardware *Design*, not HLS
- Pipeline staging, clock gating, hierarchy etc. *implied*

This research is sponsored by Google under Google Summer of Code 2020

kunal ghosh (vlsisystemdesign.com) • 1st Co-Founder at VLSI System Design(VSD) 1w • Edited • 1

RISC-V workshop - 2 cool things happened **Calista Redmond** did workshop Closure call and Youngest participant Niel Josiah was 12years

Isn't this the best way to close the year 2020? A wonderful hands-on workshop, with participants from over 13 time-zo collectively working day/night to build their own RISC-V pip lined CPU from scratch in matter of just "Thirty Hours" and on their way to get their core listed on riscv.org

After the horrible situation created all over world by Covid, t really a moment of achievement that needs to be celebratc which gives a clear message, whatever the situation may be am gonna rise and win. That's exactly what all participants f the end of workshop. They rose and won

All the best to all participants from all 4 RISC-V workshops conducted this year. Let's call it a day.

Thanks **Steve Hoover**, **Shivam Potdar**, **Shivani Shah** and **VI Jain** for your 24/7 support. This would not have been possil without.

Year 2021 - Wait for something exciting - **Gautham Pai** Be r

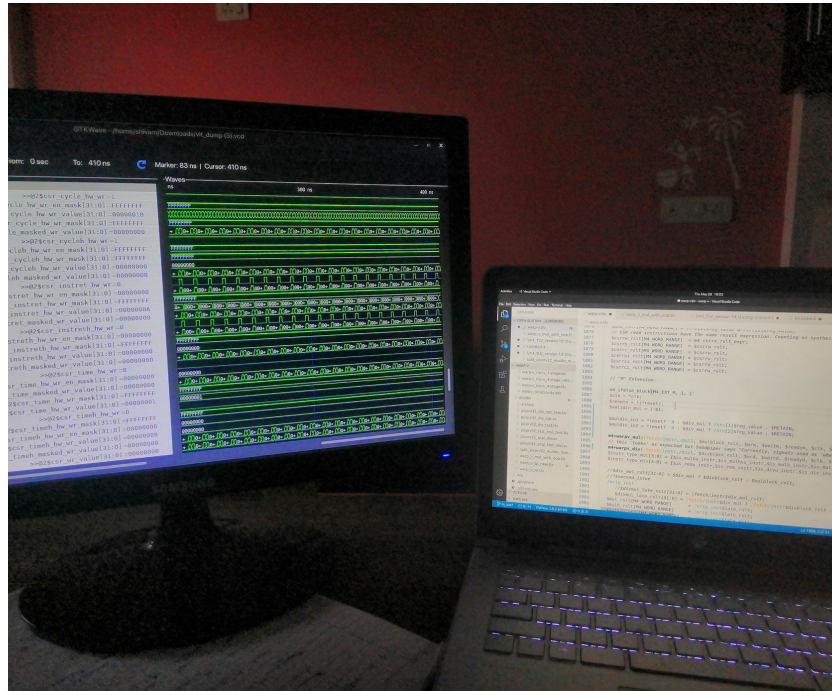
4 replies

Also sent to the channel

Kunal 15 hours ago
 Congratulations @Niel Josiah Really glad you did it. Though, I feel you should spend more time playing in fields 😊 and use free time in polishing what you are passionate about. Keep it up and continue exploring digital electronics. All the best

Razvan Ionescu 14 hours ago
 Great Niel! BTW, how old are you?

Niel Josiah 2 hours ago
 12 years old



Google LLC
 1600 Amphitheatre Parkway
 Mountain View CA 94043
 650 253-0000 main
[google.com](https://www.google.com)

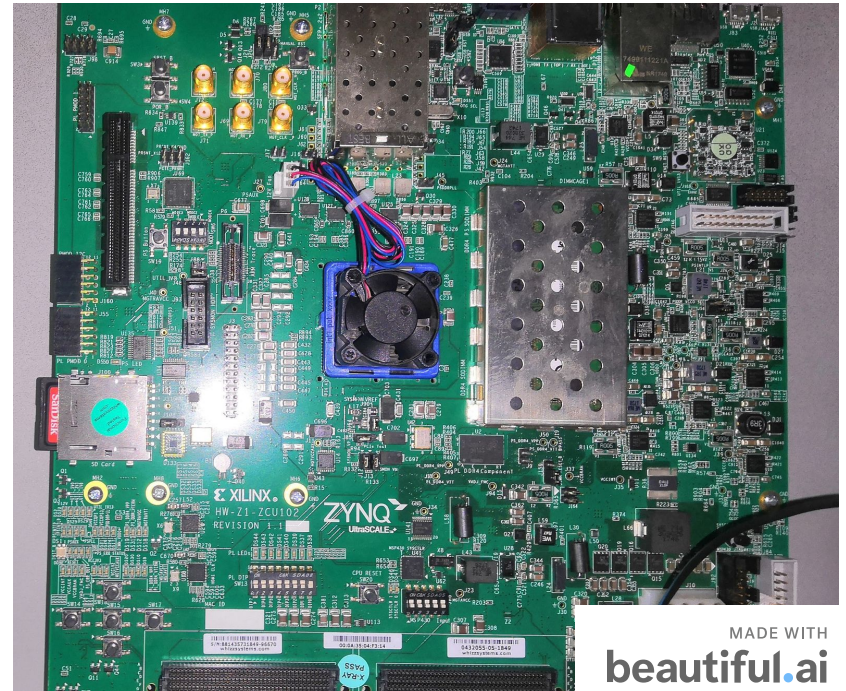
September 9, 2020

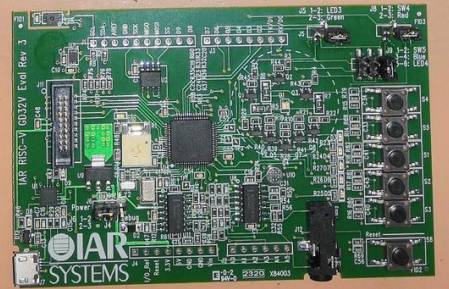
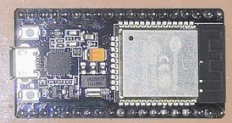
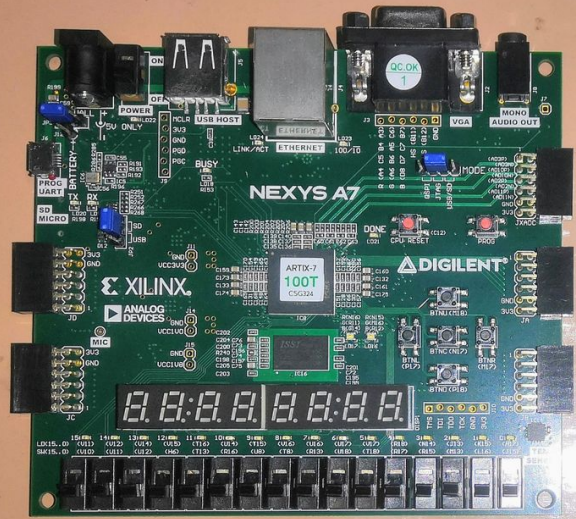
To Whom It May Concern:

Google is pleased to inform you that Shivam Potdar has successfully completed Google Summer of Code 2020, a program which connects students with mentors for 3 months to develop open source software. Each year many students apply to participate with only a portion of them being accepted into the program, and not every student finishes the program successfully.

Shivam was accepted into the program by, and developed open source software for, Free and Open Source Silicon Foundation beginning June 1, 2020 and ending on August 24, 2020. Over that period, they passed each of the three evaluations conducted by their mentor.

More information on Shivam's project can be found at:







Career Options

Career Options

- MS / PhD
- MTech / MS (R)
- Management
- Industry
- UPSC / IES / Defence
- Startup
- Something else...

The background of the slide features a dark blue, starry night sky. In the foreground, the silhouettes of two people are shown climbing a rocky cliff. One person is higher up, leaning forward to assist the other who is lower down. The scene is set against a backdrop of distant, hazy mountains and a body of water, creating a sense of adventure and teamwork.

General Tips

General Tips

- **So many areas! What do I choose?**

- “Pehle istemaal kare fir vishwas kare :)”
- Explore everything!

- **Does GPA matter?**

- For your future university / employer - maybe
- For Sharma ji - NO!

- **Core vs Software**

- Am I bound by being in some branch to its fields? NO!
- My whole portfolio is in the intersection of ECE and CSE (w.r.t NITK curriculum)

- **Knowledge**

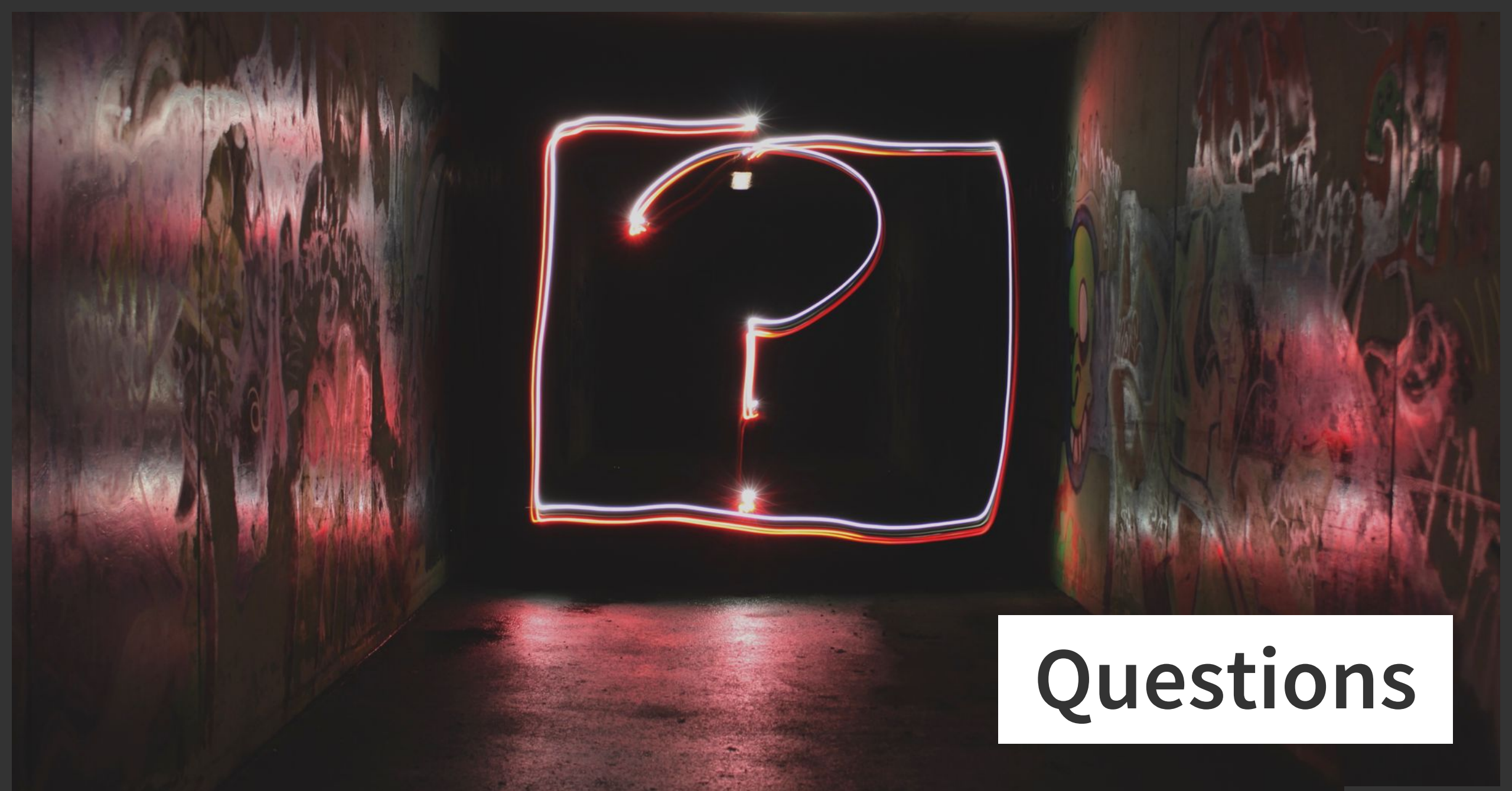
- “Chaaro taraf gyaan bat raha hai, jahan se mile lapet lo” - Baba Ranchoddas Chanchhad
- Coursera, YouTube, NPTEL, edX, MIT OCW, Udemy

- **Experience**

Research or Industry? Startup or MNC? Paid or Unpaid?
Work matters!

- **Think Out-of-the-box**

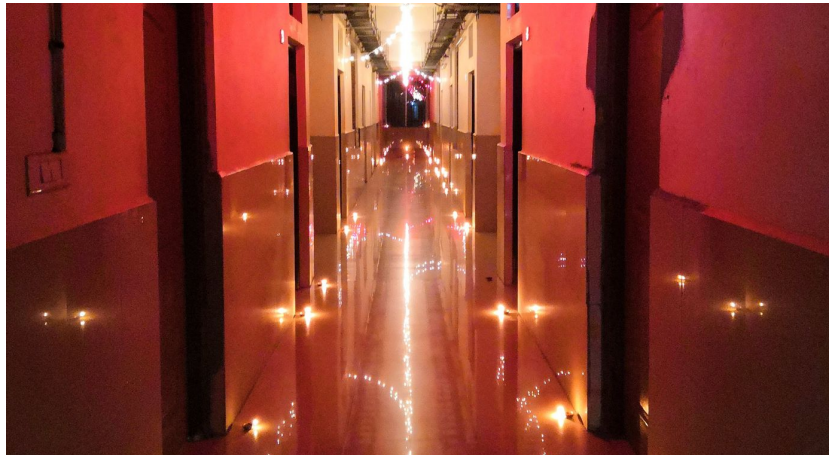
Always find ways of connecting things and doing what no one else does!



Questions



HAVE FUN!










Shivam Potdar

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