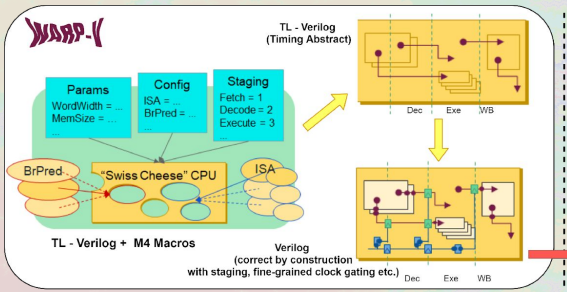
DAC YF

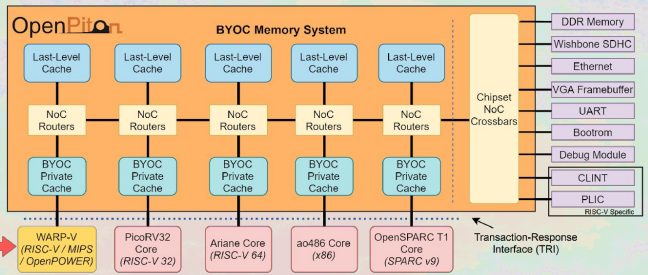
Flexible Manycore CPU Design with TL-Verilog

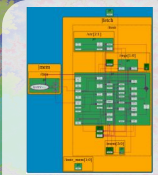
Shivam Potdar (YF), Steve Hoover, Jonathan Balkind (Mentors)

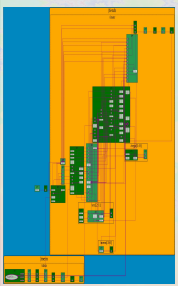
Flexible and Configurable CPU Microarchitecture



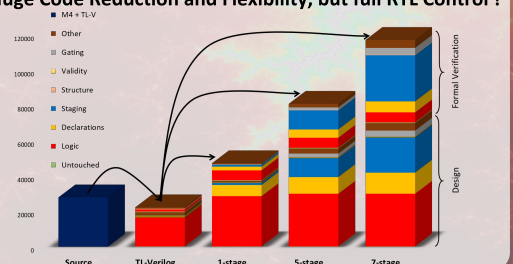
Flexible and Scalable Uncore







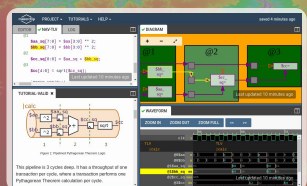
Huge Code Reduction and Flexibility, but full RTL Control !

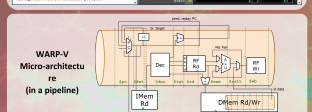


Key Takeaways :

- Demonstrates large-scale design in new Verilog-compatible transaction-level design and formal verification methodology
- Hardware *Design,* not HLS
- Pipeline staging, clock gating, hierarchy etc. *implied*

This research is sponsored by Google under Google Summer of Code 2020





shivampotdar99@gmail.com

GitHub Links and My Portfolio - https://linktr.ee/shivampotdar